REMARKS

In response to the action of March 21, 2007, applicants asks that all claims be allowed in view of the amendments to the claims and the following remarks.

Claims 3-8, 11-14 and 16-33 are currently pending, of which claims 3, 6, 11-14, 16, 19, 22 and 26 are independent. Claims 3, 6, 16, 19 have been amended. Support for these amendments may be found in the application at, for example, page 10, lines 26-34 and FIGS. 2A and 3A. No new matter has been introduced.

Applicant acknowledges with appreciation the Examiner's indication that claims 30-33 would be allowable if written in independent form including all limitations of the base claim and any intervening claims. Applicant has not amended these claims at this time.

Rejection Under 35 U.S.C. § 112, Second Paragraph

Claims 3-5 and 16-18 have been rejected under 35 U.S.C. §112, second paragraph, as being indefinite. Applicant believes the amendment of independent claims 3 and 16 addresses all of the Examiner's concerns. Accordingly, applicant respectfully requests reconsideration and withdrawal of this rejection of claims 3 and 16, and their respective dependent claims 4, 5, 17 and 18.

Rejections Under 35 U.S.C. § 103

Claims 3-8, 11-14 and 16-29 have been rejected as being unpatentable over Stewart (U.S. Patent No. 5,952,789) in view of Yamagishi (U.S. Patent No. 6,501,466). Applicant requests reconsideration and withdrawal of the rejection because neither Stewart, Yamagishi, nor any combination of the references, describes or suggests the subject matter of the independent claims.

Independent Claims 3 and 16

Claim 3 recites a current source circuit that includes, among other elements, a first transistor, a second transistor, and a capacitor element connected to the gate electrodes of the

first transistor and the second transistor. The circuit also includes a power source line connected to one end of the capacitor element and a current source line connected to the other end of the capacitor element. The current source circuit also includes means for supplying electric charges held in the capacitor element to the gate electrodes of the first and second transistors. The first and second transistors are connected in a parallel connection state when storing electric charges in the capacitor element.

Stewart discloses a switching power line that is connected to a capacitor and a current source that is connected to transistors T1 and T2, as shown in FIG. 5. As noted by the action with regard to claim 11, Stewart does not disclose that the first and second transistors are connected in parallel. See action at page 5, lines 3-4. See also Stewart at FIG. 5 (showing the connection state between the TFT 1 and the TFT 2 is a series connection state). As such, Stewart does not describe or suggest a current source circuit where the first and second transistors are connected in a parallel connection state when storing electric charges in the capacitor element, as recited by claim 3.

Yamagishi is said to disclose in FIG. 1 "an active matrix type display apparatus and drive circuit thereof comprising the two transistors TFT1 and TFT2 [that] are connected in parallel." See action at page 5, lines 3-4. Applicant respectfully disagrees. Yamagishi indicates that "the picture element drive circuit [in FIG. 1] includes a conversion thin film transistor TFT1, where the signal current flows through the transistor TFT1, and a drive thin film transistor TFT2 for controlling the drive current flowing through a light emitting device...." See Yamagishi at col. 7, lines 62-67 (referring to FIG. 1). As shown in FIG. 1, TFT1 and TFT2 are not connected in parallel. Instead, as shown in FIG. 1, TFT1 is connected between Vdd and terminals of TFT3 and TFT4, while TFT2 is connected between Vdd and the OLED. Accordingly, Yamagishi does not describe or suggest a parallel connection between TFT1 and TFT2.

Accordingly, neither Stewart, Yamagishi, nor any proper combination of the references, describes or suggests a parallel connection between the first and second transistors. Accordingly, Stewart and Yamagishi, alone or in combination, do not describe or suggest a current source circuit where the first and second transistors are connected in a parallel connection

state when storing electric charges in the capacitor element, as recited by claim 3. Therefore, for at least these reasons, applicant requests reconsideration and withdrawal of the rejection of claim 3 and its dependent claims 4 and 5.

Independent claim 16, similarly to claim 3, recites a current source circuit including a first transistor and a second transistor, where the first and second transistors are connected in a parallel connection state when storing electric charges in the capacitor element. Accordingly, for at least the reasons noted above with respect to claim 3, applicant requests reconsideration and withdrawal of the rejection of claim 16 and its dependent claims 17 and 18.

Independent Claims 6 and 19

Independent claim 6 recites a current source circuit that includes, among other elements, a first transistor, a second transistor, a third transistor, and a capacitor element connected to the gate electrodes of the first transistor, the second transistor and the third transistor.

The action acknowledges that Stewart does not disclose a capacitor element connected to the gate electrodes of the first transistor and the second transistor. See action at page 3, lines 14-15. As such, Stewart cannot, and does not, disclose a capacitor element connected to the gate electrodes of the first transistor, the second transistor and the third transistor.

Yamigishi is said to disclose in FIG. 1 a capacitor that is connected to both the gate electrodes of TFT 1 and TFT 2. However, Yamigishi does not disclose a capacitor connected to the gate electrode of a third transistor. As such, Yamigishi does not remedy the failure of Stewart to describe or suggest a capacitor element connected to the gate electrodes of the first transistor, the second transistor and the third transistor.

Accordingly, for at least these reasons, applicant requests reconsideration and withdrawal of the rejection of claim 6 and its dependent claims 7 and 8.

Claim 19, similarly to claim 6, recites a current source circuit that includes, among other elements, a first transistor, a second transistor, a third transistor, and a capacitor element connected to the gate electrodes of the first transistor, the second transistor and the third transistor. Accordingly, for at least the reasons noted above with respect to claim 6, applicant

requests reconsideration and withdrawal of the rejection of claim 19 and its dependent claims 20 and 21.

Applicant respectfully notes that the remarks presented above with respect to claims 6 and 19 were made in the prior reply. See Applicant's reply to action of September 14, 2006 at page 12. The present action does not address these prior remarks. In the event that the Examiner chooses to maintain this rejection, applicant requests that the Examiner provide a meaningful explanation of whatever the Examiner determines to be deficient about these remarks.

Independent Claims 11-14

Independent claim 11 recites a method for driving a current source circuit having a first transistor and a second transistor. The method includes feeding current supplied from the power source line to the current course line through the first transition and the second transistor, which are connected in parallel with each other. As described previously with respect to claim 3, neither Stewart, Yamagishi, nor any proper combination of the references, describes or suggests a parallel connection between the first and second transistors. As such, neither Stewart, Yamagishi, nor any proper combination of the references, describes or suggests feeding current supplied from the power source line to the current course line through the first transition and the second transistor, which are connected in parallel with each other, as recited by claim 11.

In addition, Stewart does not describe or suggest feeding current supplied from the power source line to the current source line through the first transistor and the second transistor (whether connected in parallel or otherwise), as recited by claim 11. See, e.g., Stewart at FIG. 5. Yamagishi does not remedy this failure of Stewart.

Moreover, each of Stewart and Yamagishi disclose only one type of connection between the first and second transistors. Thus, even if Yamagishi had disclosed connecting the first and second transistors in parallel, one skilled in the art would not have been motivated to combine such parallel connected transistors with Stewart's connection of the first and second transistors in series. As such, one skilled in the art facing whatever need or problem was known in the relevant field, would not have been led to modify or combine these references in a manner

resulting in the current source circuit recited in claim 11, without first consulting applicant's disclosure. See KSR Int'l Co. v. Teleflex Inc., No. 04-1350, 550 U.S. ___, 2007 WL 1237837 (Apr. 30, 2007).

Accordingly, for at least these reasons, applicant requests reconsideration and withdrawal of the rejection of claim 11.

Claims 12, 13 and 14 each recite a method for driving a current source circuit having a first transistor and a second transistor. The methods each require that the first and second transistor are connected in parallel. Claim 12 recites connecting the first transistor and second transistor in parallel with each other when a setting operation is performed on the first transistor and second transistor. Claims 13 and 14 each recite supplying current based on the predetermined amount of voltage to the first transistor and second transistor, which are connected in parallel with each other, such that the transistors can feed a predetermined amount of current.

For at least the reasons described above with respect to claim 3, neither Stewart, Yamagishi, nor any proper combination of the references, describes or suggests a parallel connection between the first and second transistors. Because Stewart and Yamagishi do not describe or suggest a parallel connection between the first and second transistors, Stewart and Yamagishi, alone or in combination, do not describe or suggest the subject matter of claims 12-14.

Therefore, for at least these reasons, applicant requests reconsideration and withdrawal of the rejection of claims 12-14.

Applicant respectfully notes that the remarks presented above with respect to claims 11-14 were made in the prior reply. See Applicant's reply to action of September 14, 2006 at pages 12-13. The present action does not address these prior remarks. In the event that the Examiner chooses to maintain this rejection, applicant requests that the Examiner provide a meaningful explanation of whatever the Examiner determines to be deficient about these remarks.

Independent Claims 22 and 26

Independent claims 22 and 26 each recite a current source circuit including a first transistor and a second transistor, where the first and second transistors are connected in parallel with each other when the capacitor element is connected to the power source line and the current source line. The first and second transistors are connected in series with each other when a current is supplied to an element to be driven.

For at least the reasons described above with respect to claim 3, neither Stewart, Yamagishi, nor any proper combination of the references, describes or suggests a parallel connection between the first and second transistors. Because Stewart and Yamagishi do not describe or suggest a parallel connection between the first and second transistors, Stewart and Yamagishi, alone or in combination, do not describe or suggest a current source circuit including a first transistor and a second transistor, where the first and second transistors are connected in parallel with each other when the capacitor element is connected to the power source line and the current source line, and the first and second transistors are connected in series with each other when a current is supplied to an element to be driven, as recited by claims 22 and 26.

Therefore, for at least these reasons, applicant requests reconsideration and withdrawal of the rejection of claims 22 and 26 and their respective claims 23-25 and 27-29.

Applicant respectfully notes that the remarks presented with respect to claims 22 and 26 in the prior reply were not addressed in the present action. In the event that the Examiner chooses to maintain this rejection, applicant requests that the Examiner provide a meaningful explanation of whatever the Examiner determines to be deficient about these remarks.

Conclusion

Applicant submits that all claims are in condition for allowance.

It is believed that all of the pending issues have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims)

that have not been expressed. Finally, nothing in this reply should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this reply, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

No fee is believed to be due in connection with the filing of this paper on the Electronic Filing System (EFS). In the event that any fees are due, please apply any charges or credits to deposit account 06-1050.

Respectfully submitted,

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